

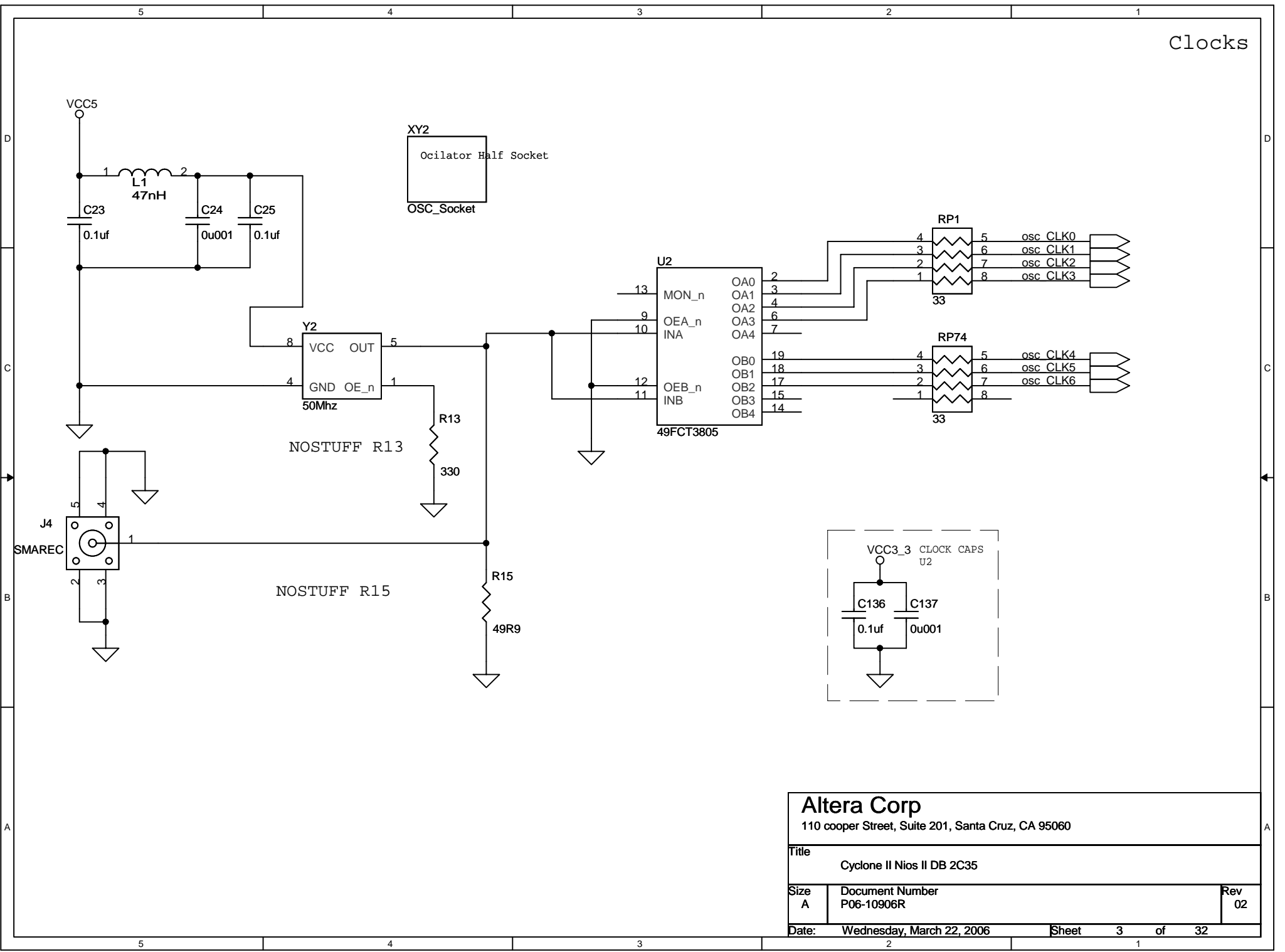
Nios Development Board

Cyclone II Edition

RoHS Rev02

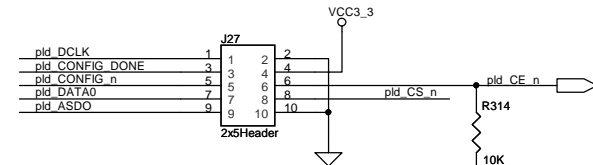
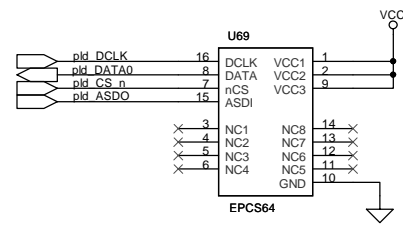
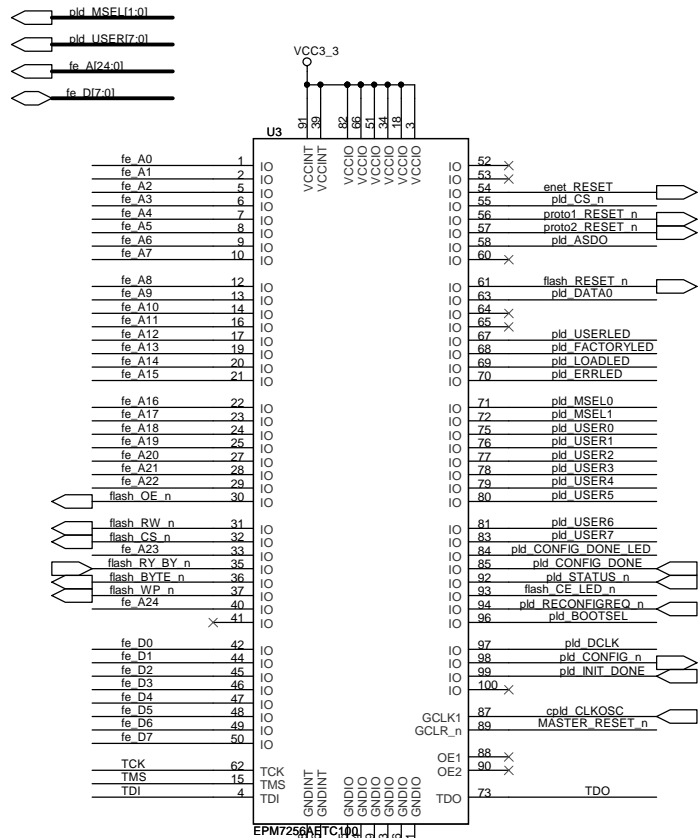
Revision History		
Date	Change Description	Rev
10/19/04	Started design	00
3/24/05	Started Rev01 of design to move the pmc_reset line and the correct the RAS and CAS lines as well as the SSRAM address lines.	01
12/22/05	Started Rev03 of design for RoHS conversion and incorporation of a few minor SPR changes.	02

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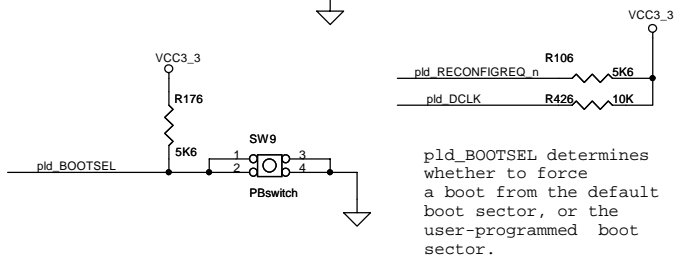
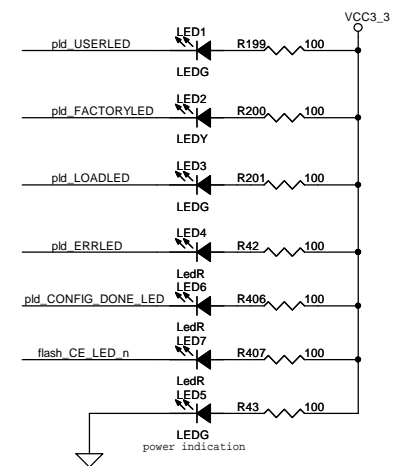
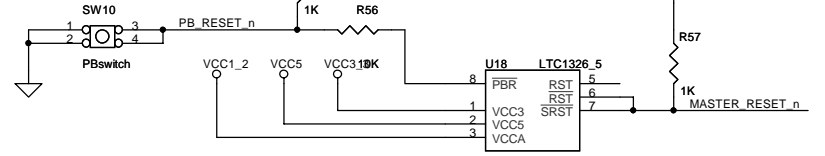


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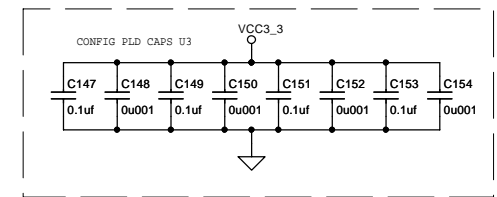
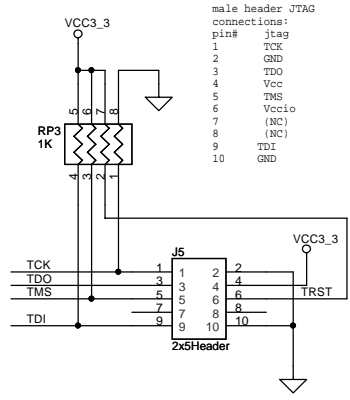
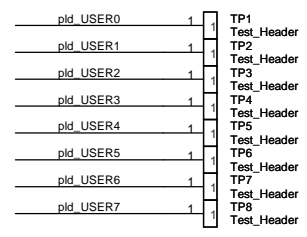
Configuration PLD



Label this button very clearly with the words. POWER ON RESET and put a box around the button and text.



NOSTUFF TP1 - 8



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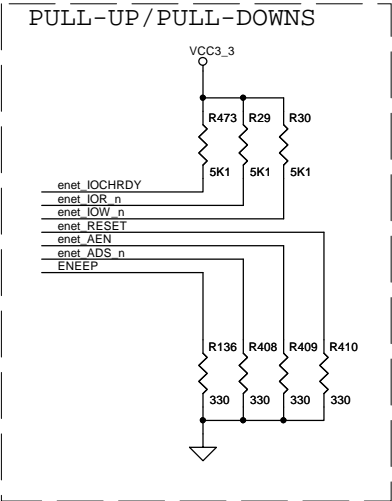
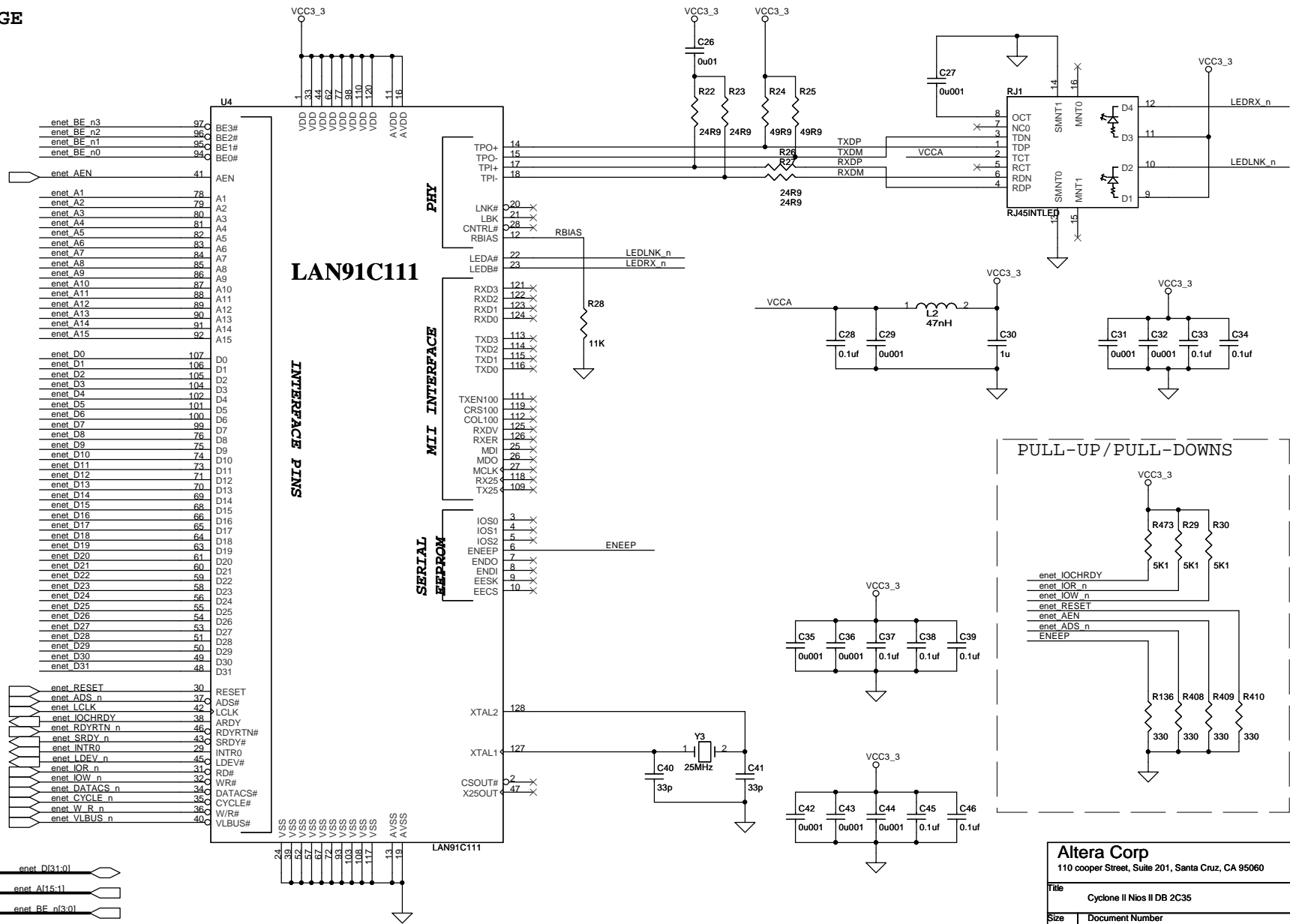
Title: Cyclone II Nios II DB 2C35

Size	Document Number	Rev
B	P06-10906R	02

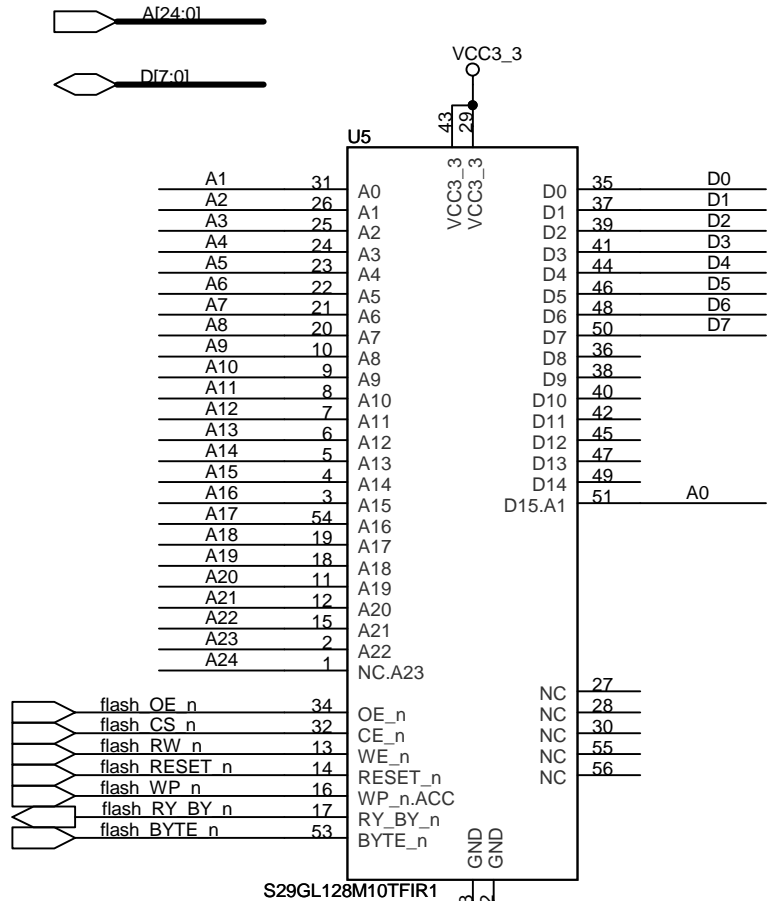
Date: Wednesday, March 22, 2006 Sheet 4 of 32

NO CHANGE

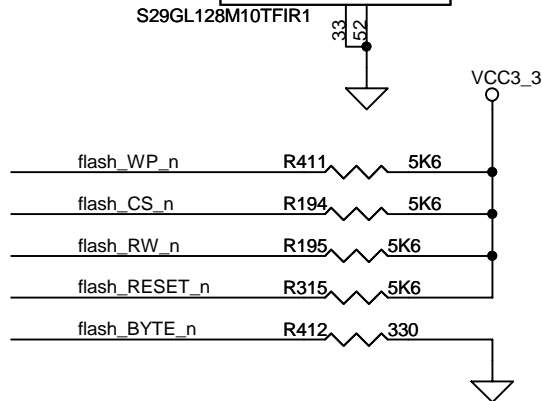
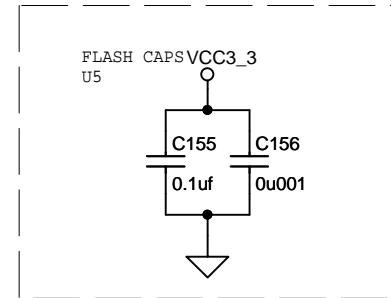
Ethernet



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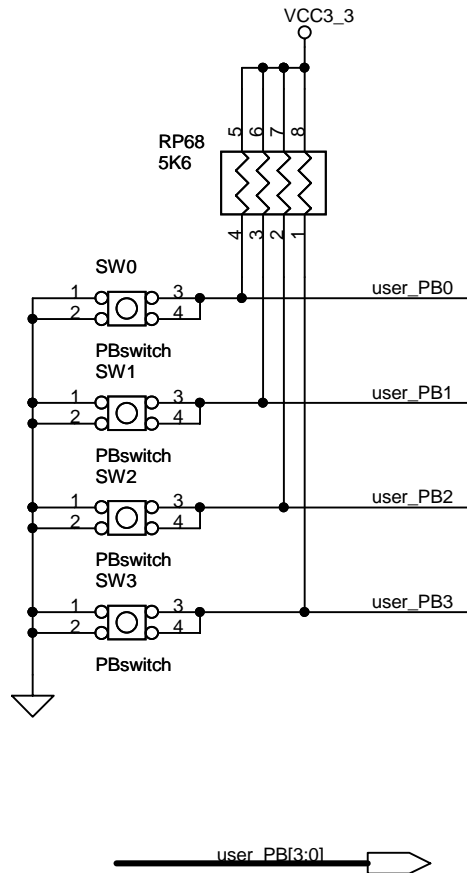
Flash chip is 16M x 8 for 16Mbytes of flash



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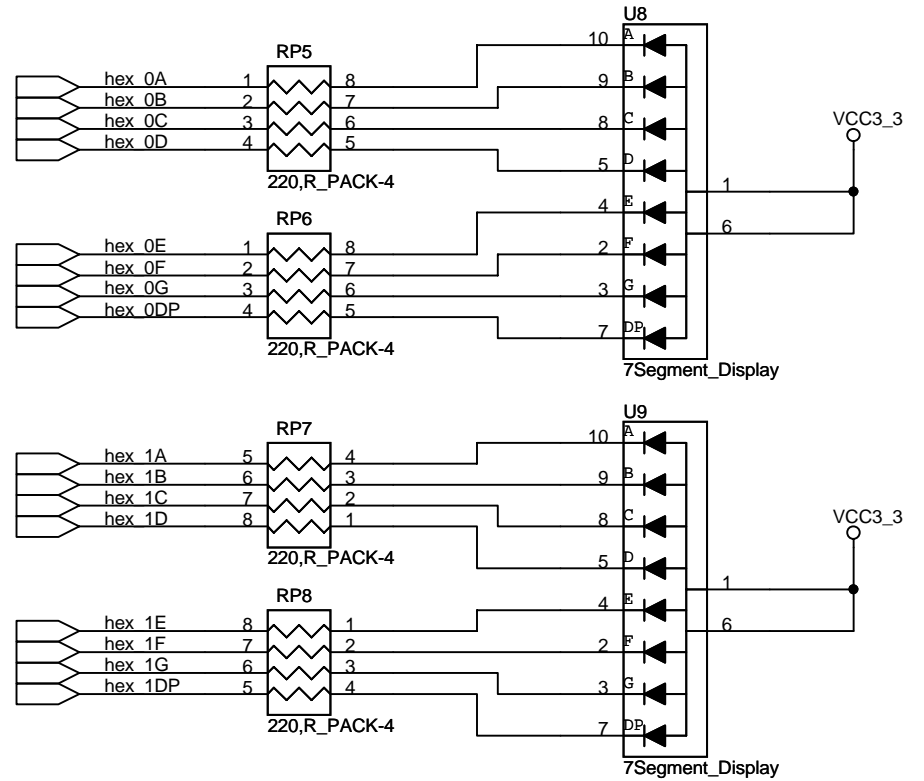
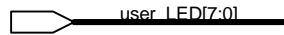
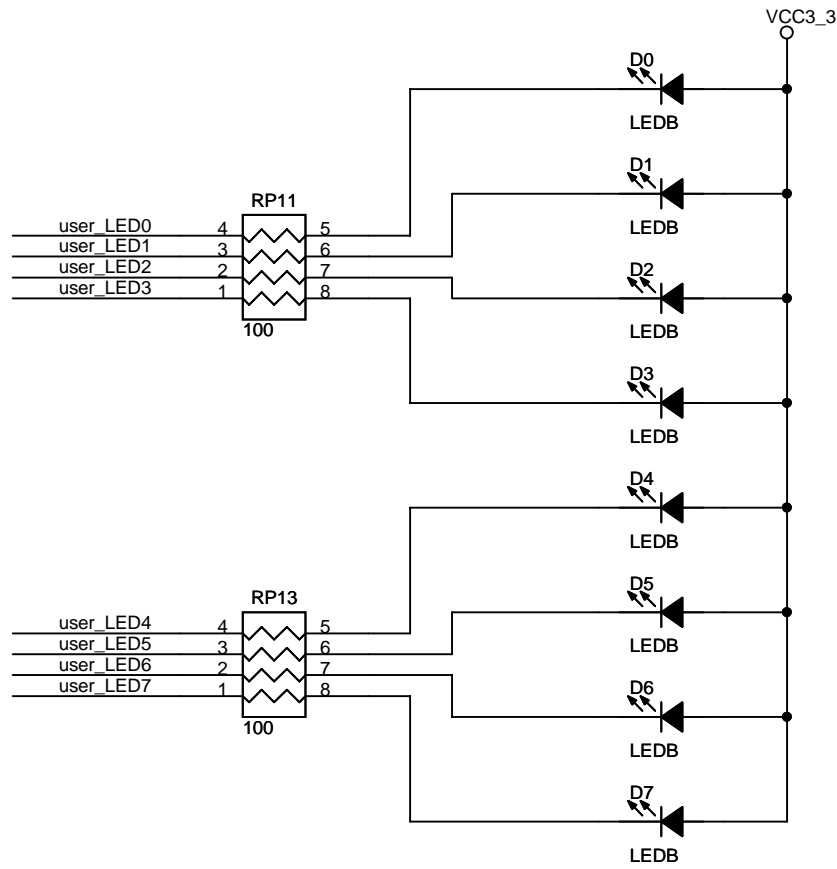
NO CHANGE

Buttons

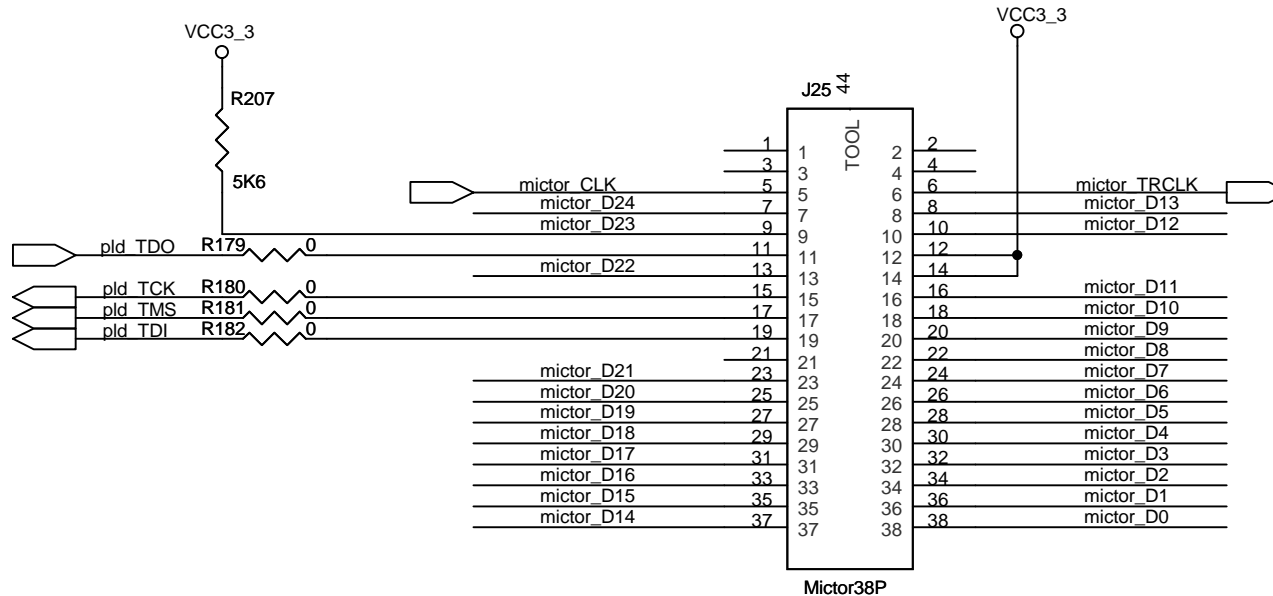


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Leds and Hex Display

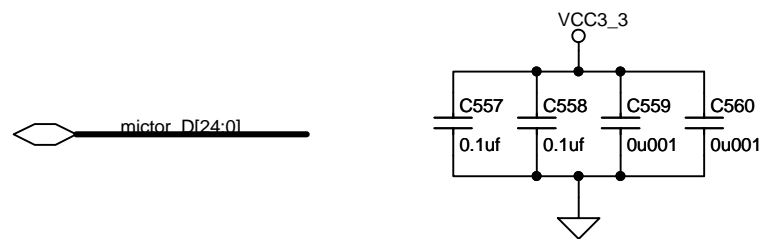


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Do not stuff R418 R419 R420 R421 R422 R423

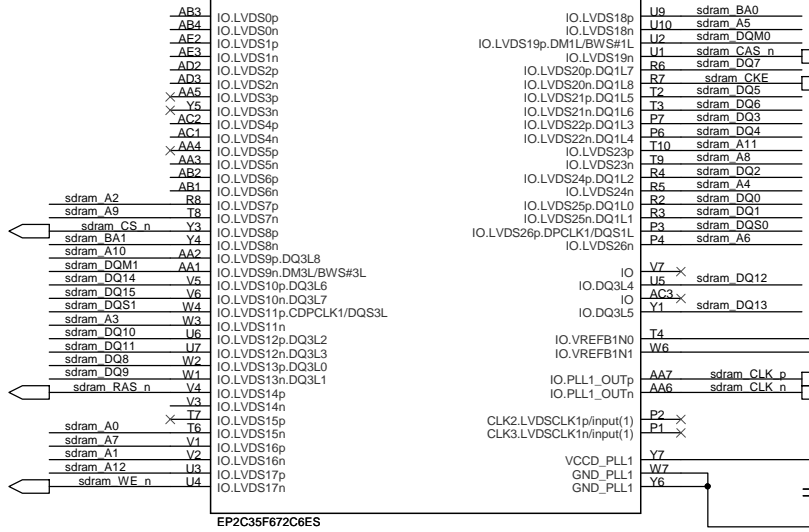
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mictor_D1		
mictor_D2	R419	100
mictor_D3		
mictor_D4	R420	100
mictor_D5		
mictor_D6	R421	100
mictor_D7		
mictor_D8	R422	100
mictor_D9		
mictor_D10	R423	100
mictor_D11		



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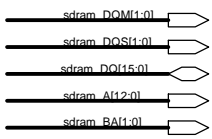
PLD Bank 1

U62A

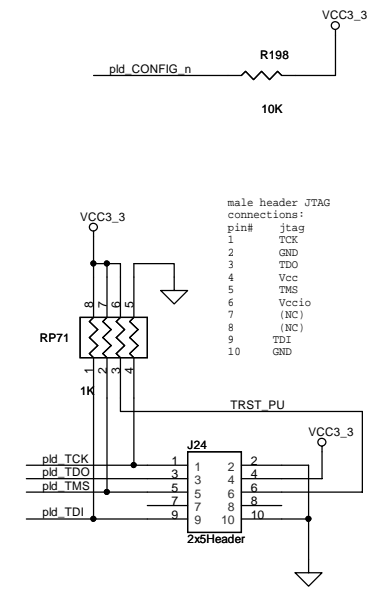
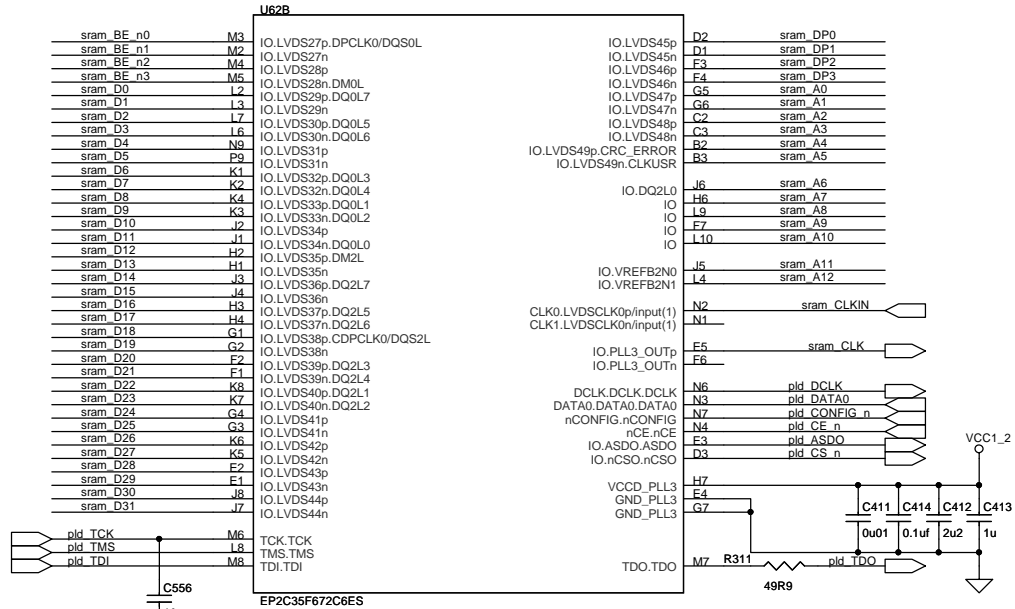


RAS and CAS signals are crossed at the top level so when the signals are assigned to pins in Quartus CAS_n should be assigned to pin V4

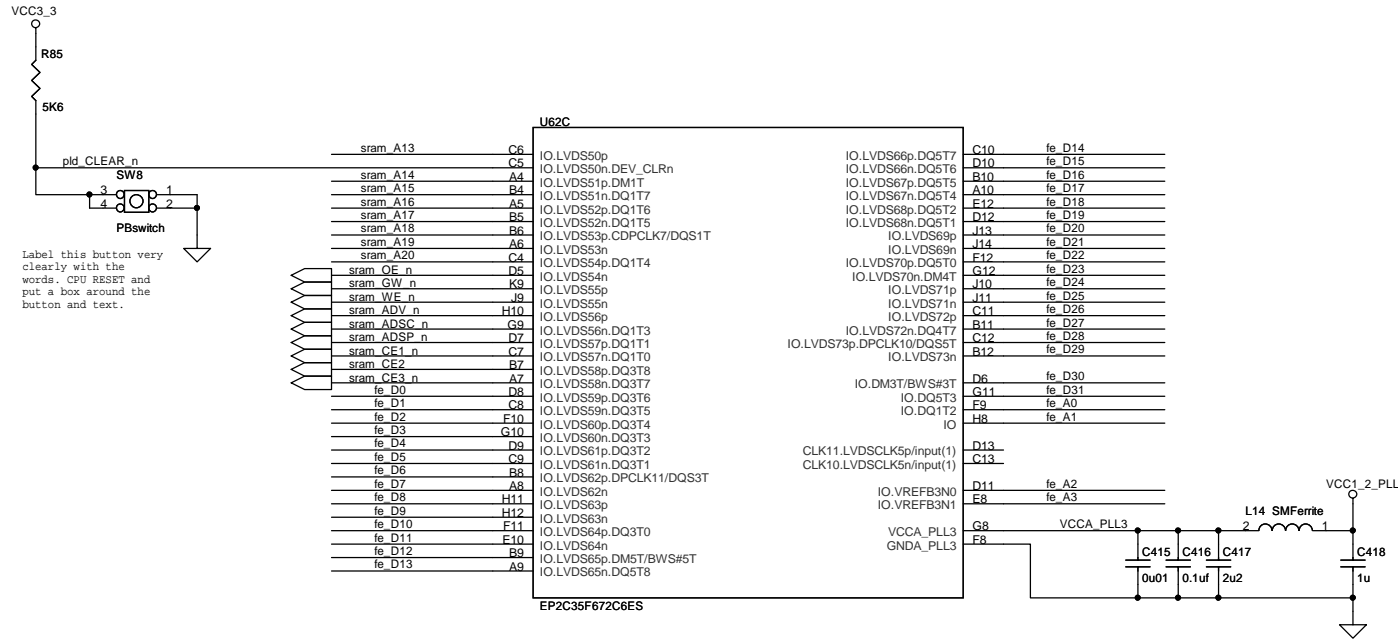
RAS and CAS signals are crossed at the top level so when the signals are assigned to pins in Quartus CAS_n should be assigned to pin U1



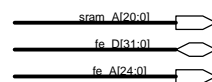
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PLD Bank 3

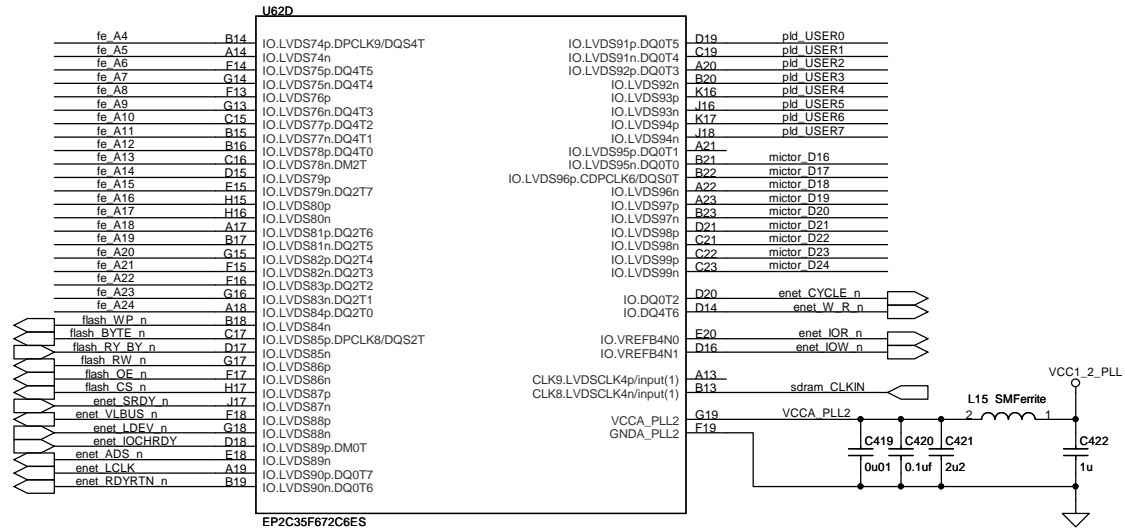


Label this button very clearly with the words, CPU RESET and put a box around the button and text.

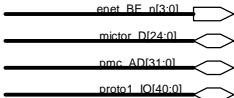
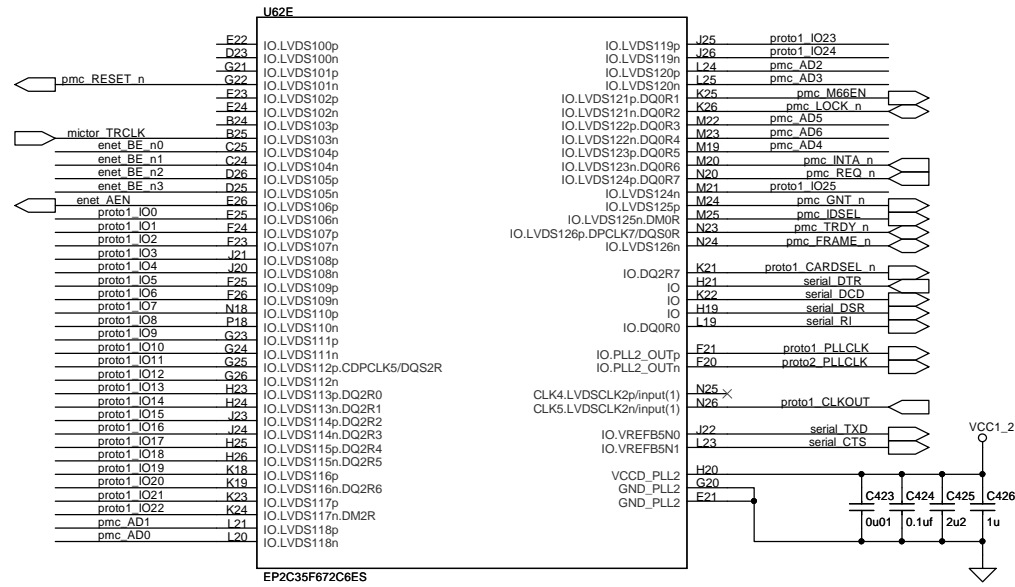


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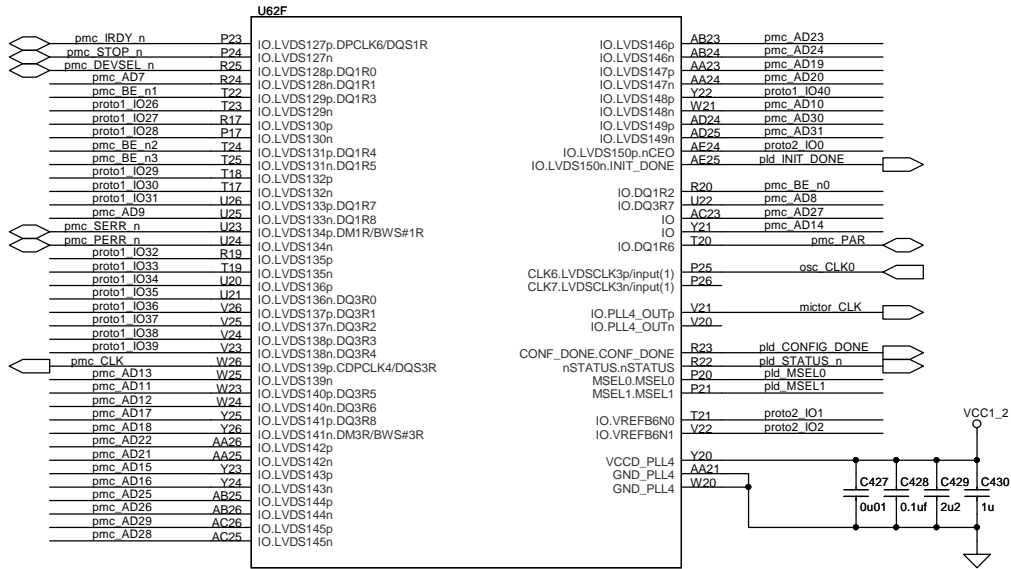
PLD Bank 4



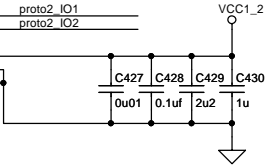
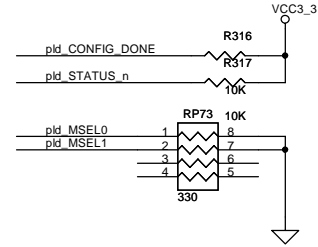
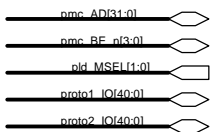
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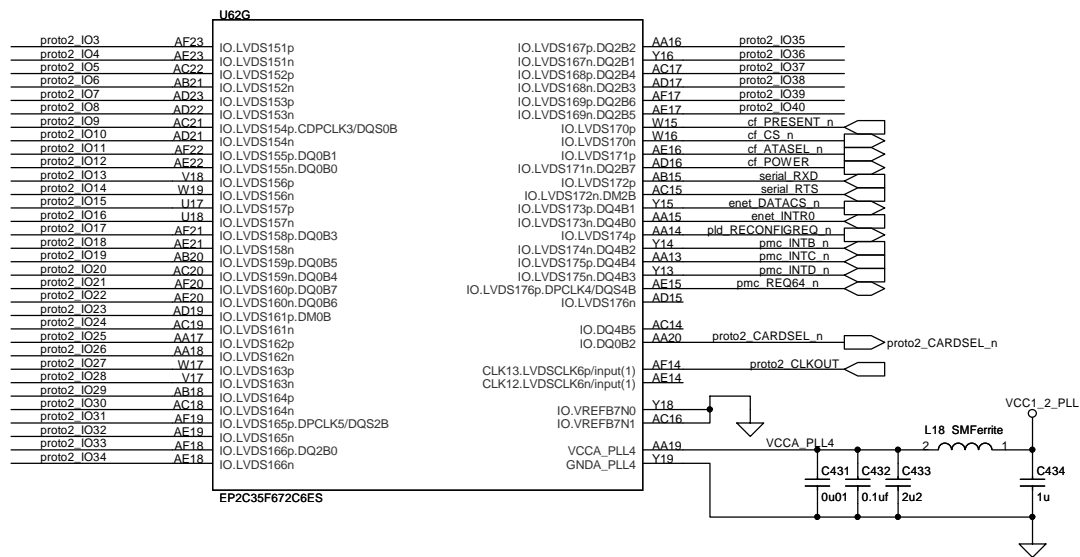
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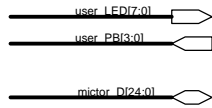
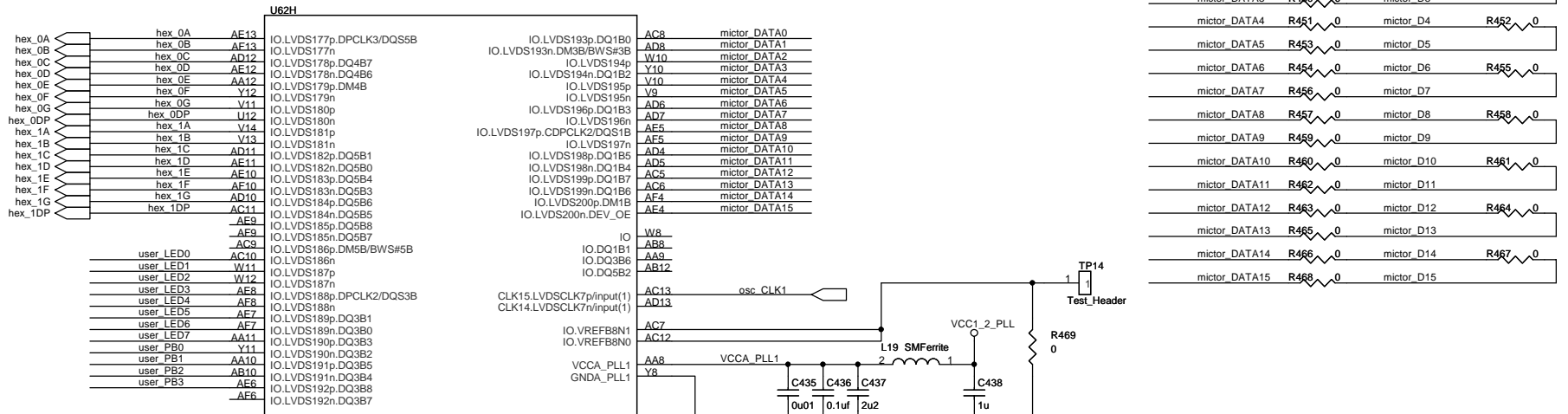
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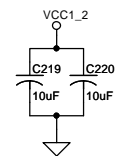
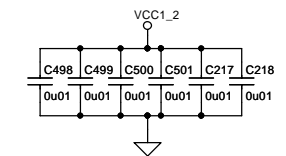
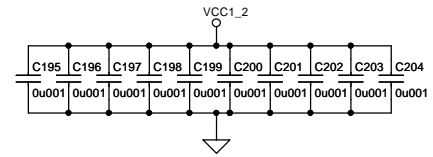
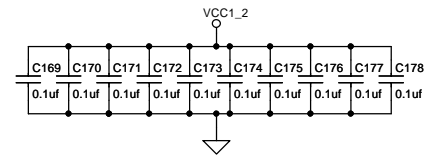
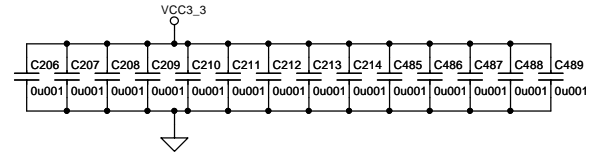
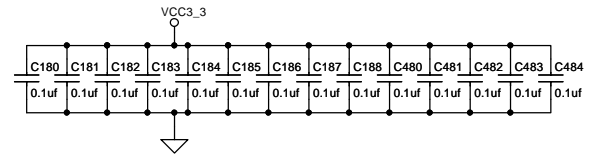
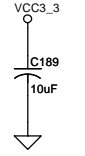
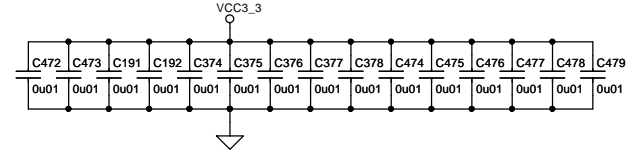
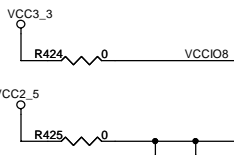
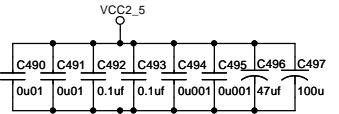
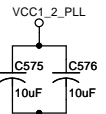
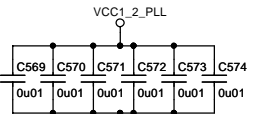
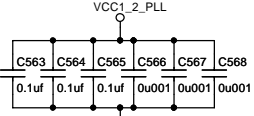
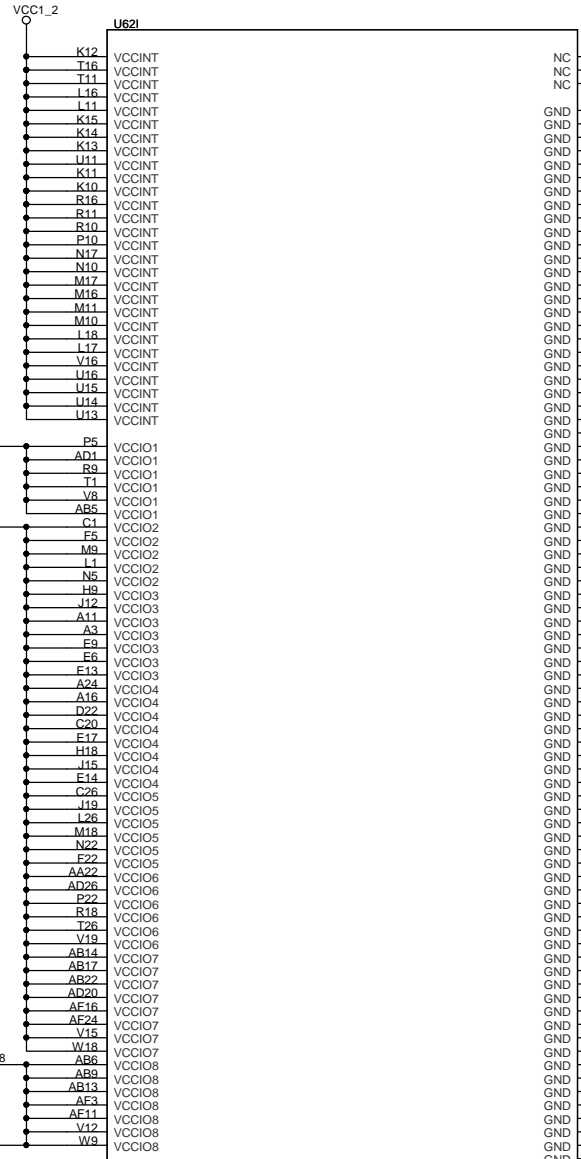
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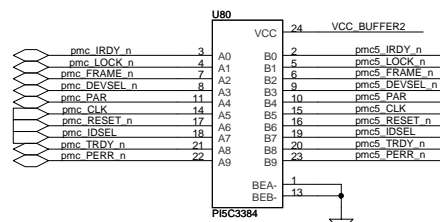
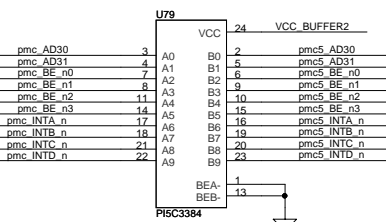
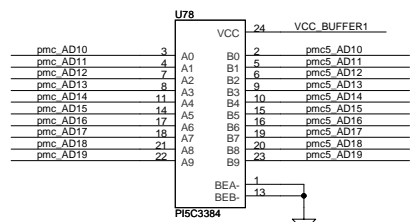
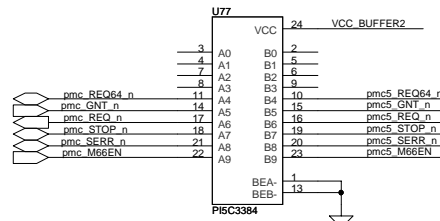
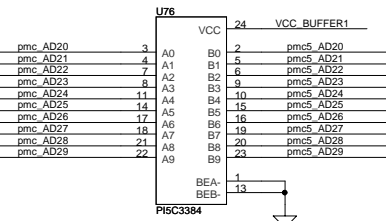
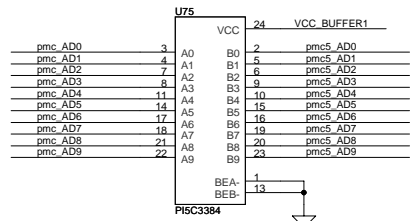
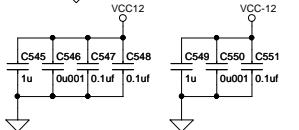
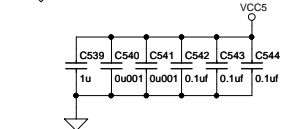
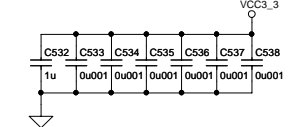
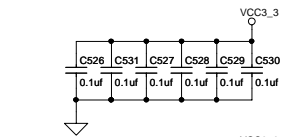
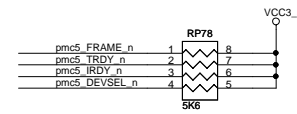
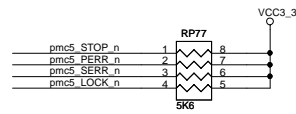
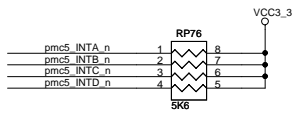
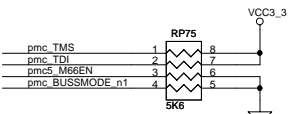
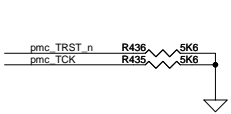
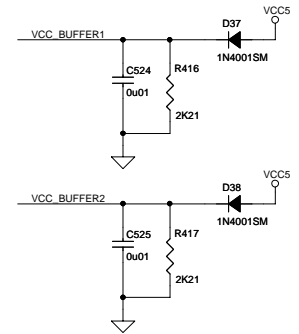
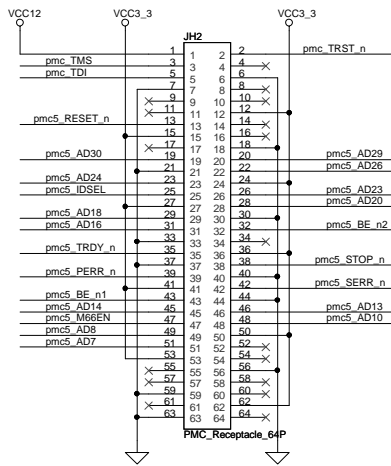
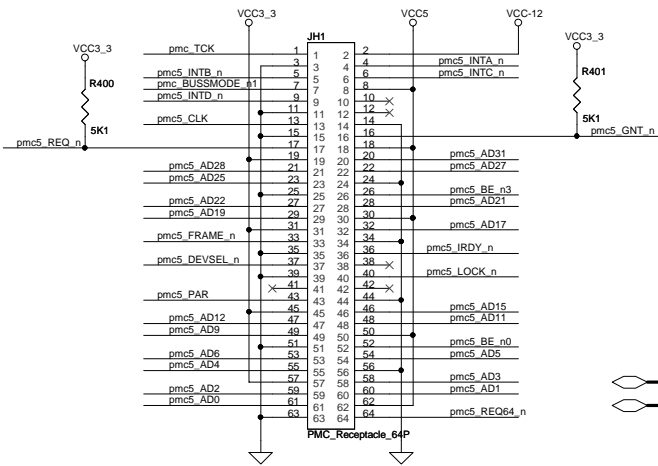
PLD Bank 8

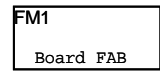
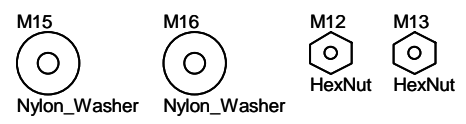
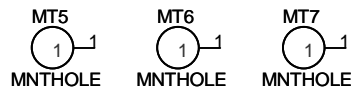
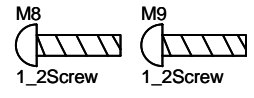
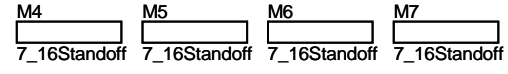
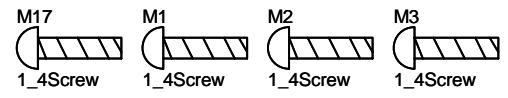
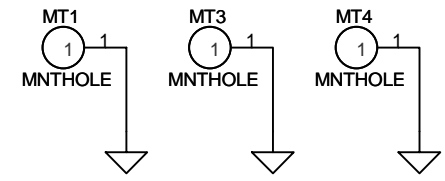
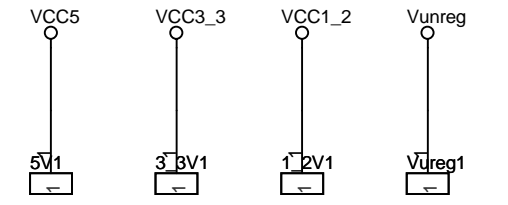
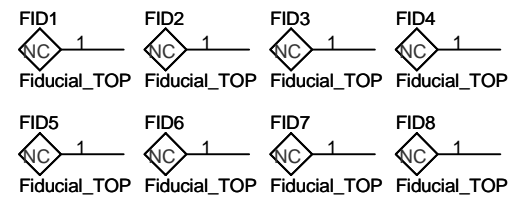
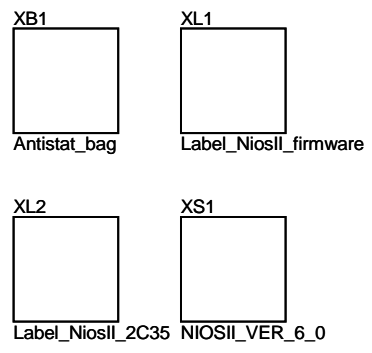
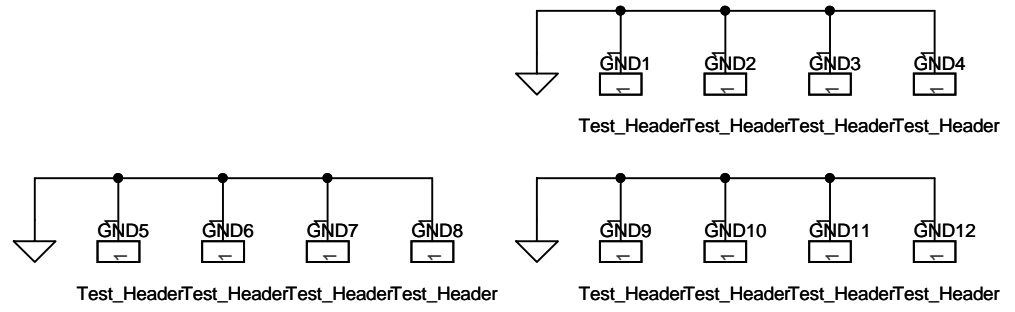
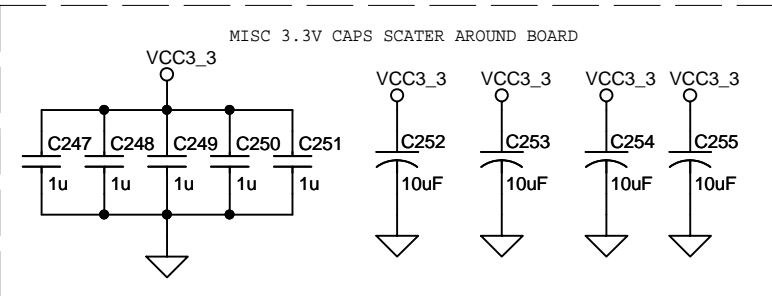
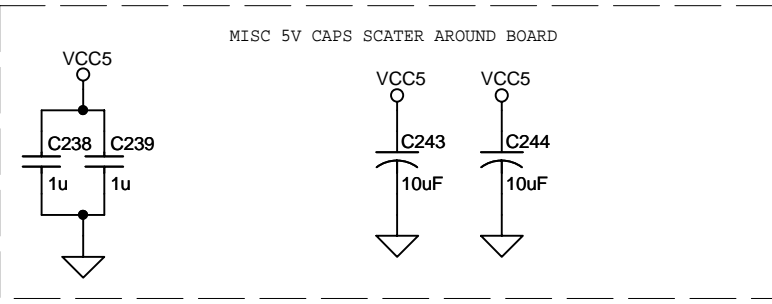


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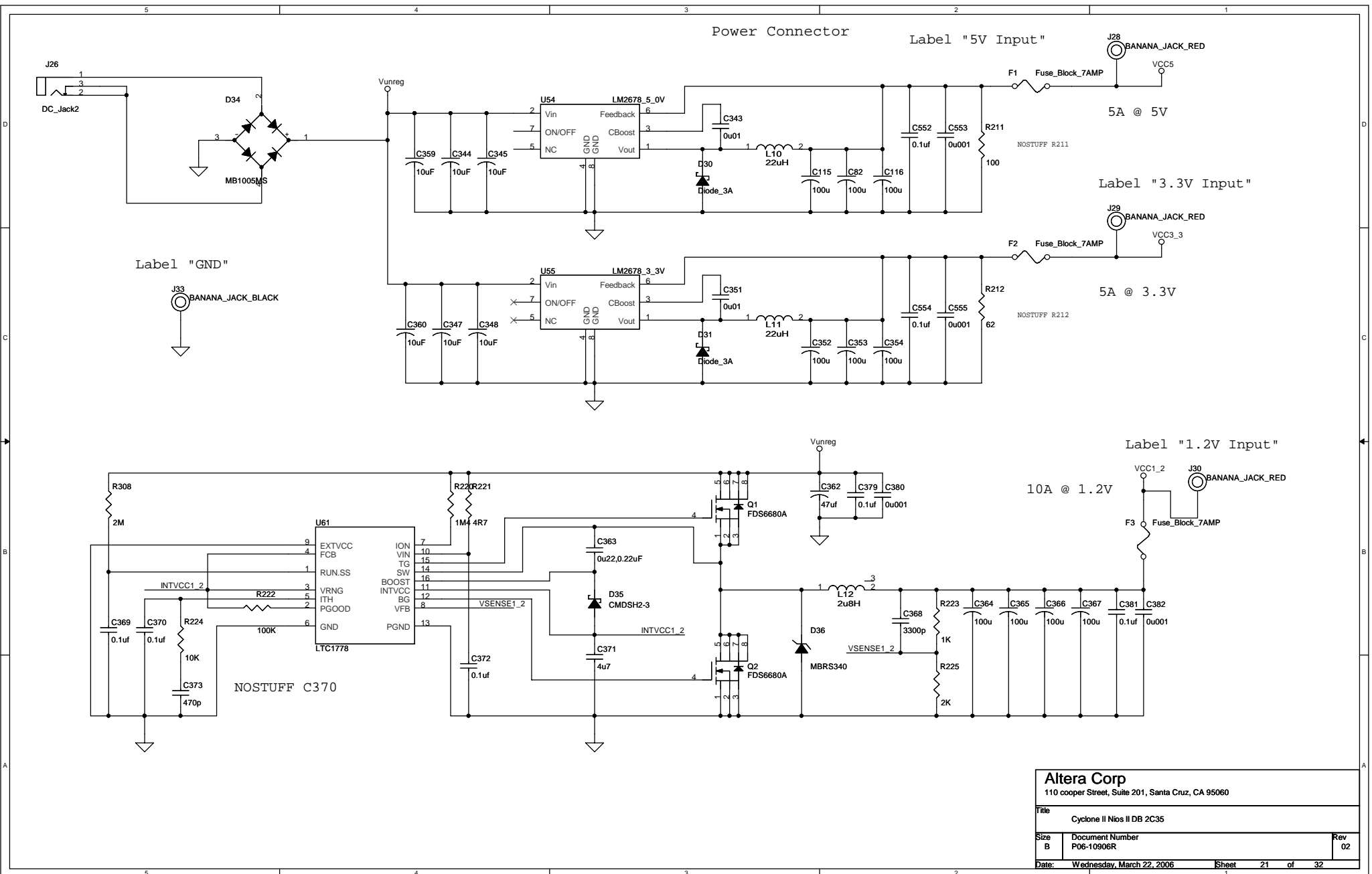
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CycloneII_NiosII_DB_2C35

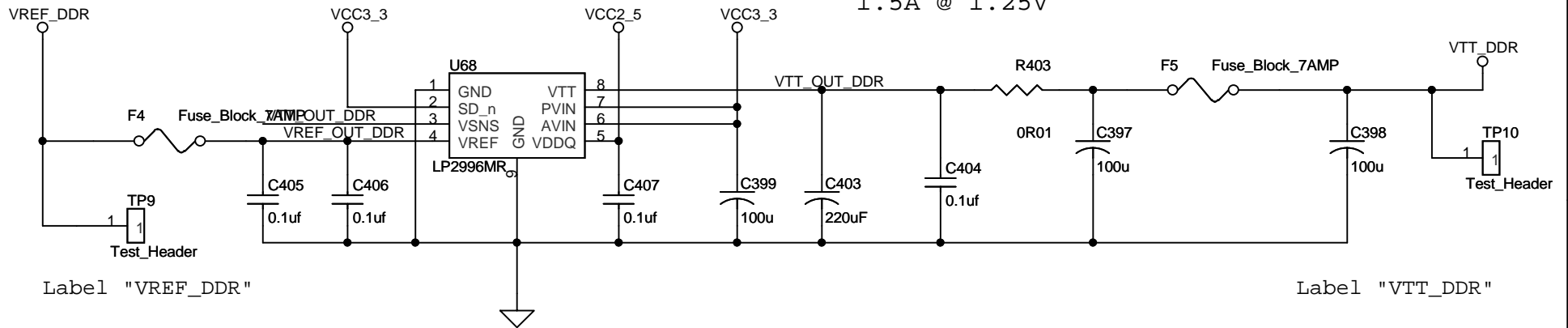
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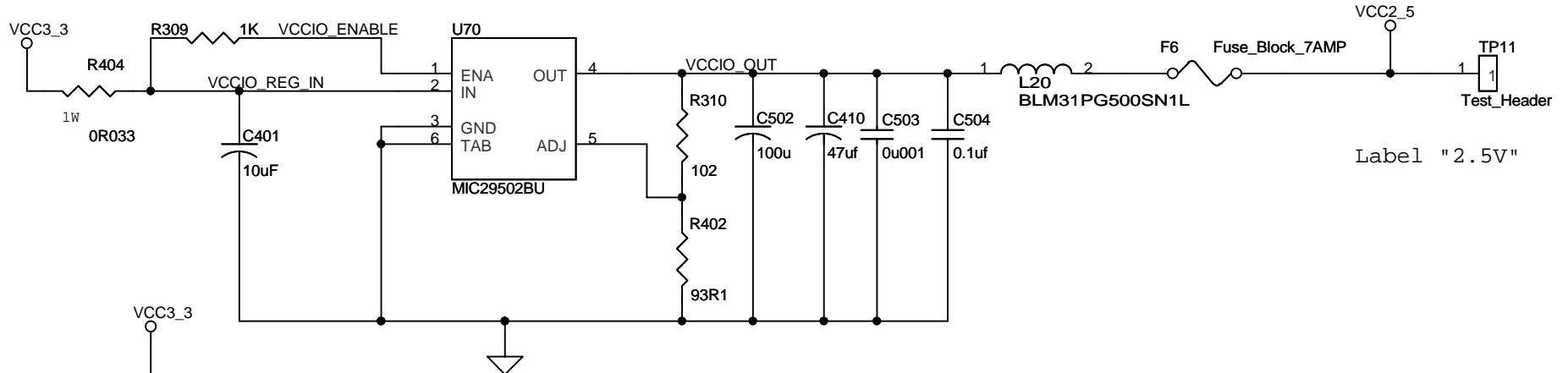
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Reset and Test headers

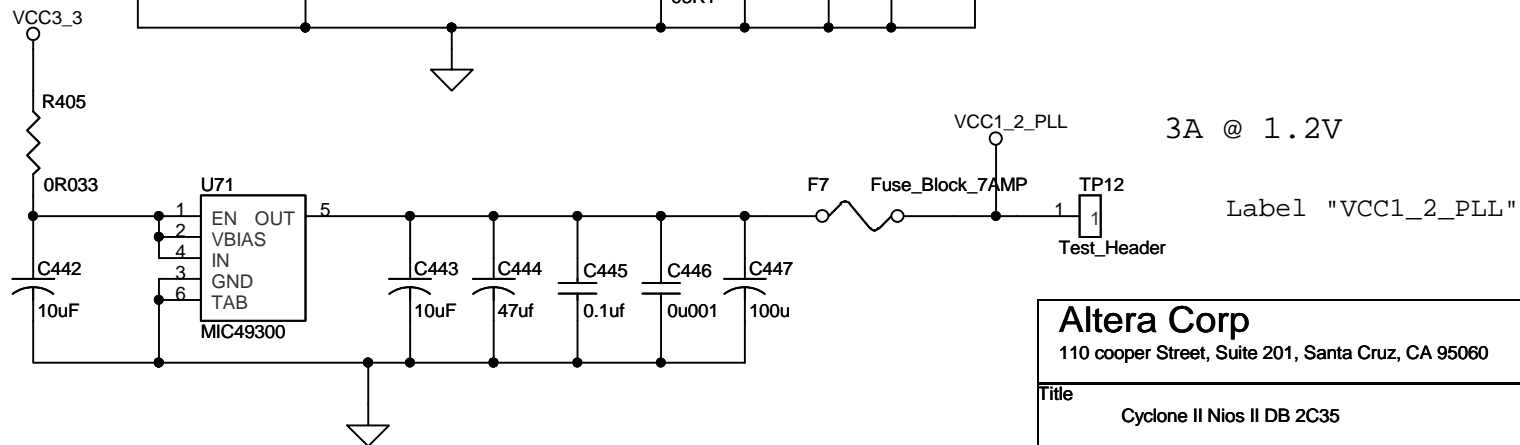
1.5A @ 1.25V



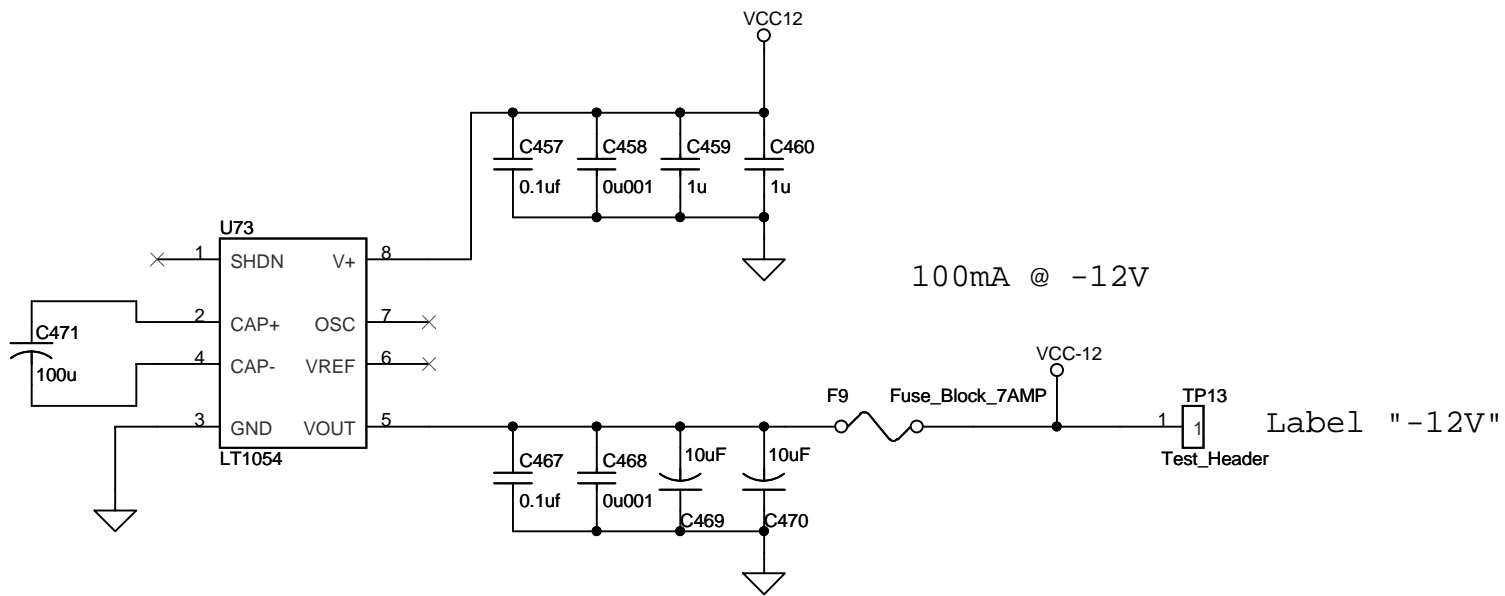
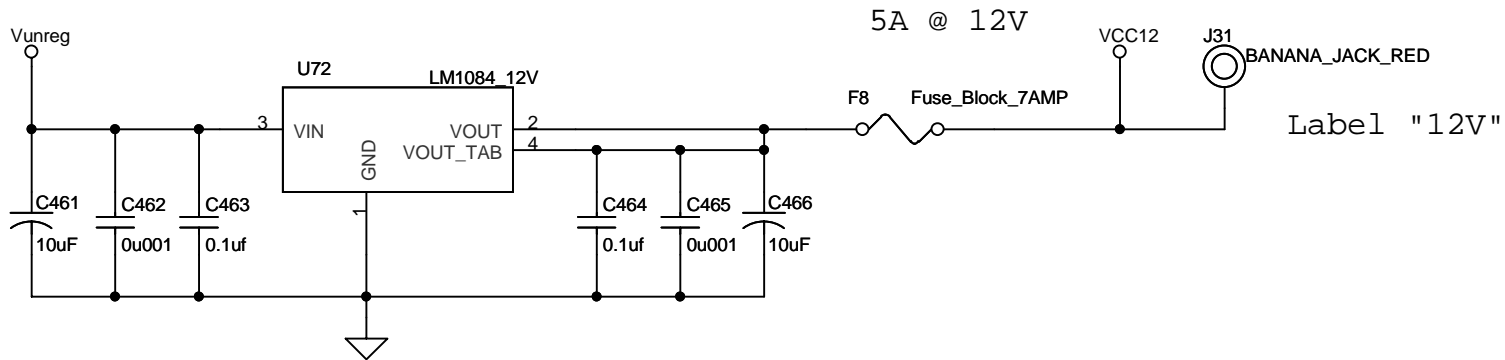
5A @ 2.5V



3A @ 1.2V



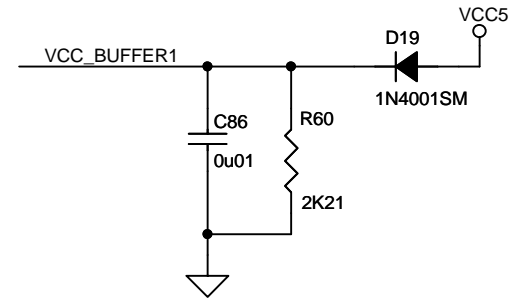
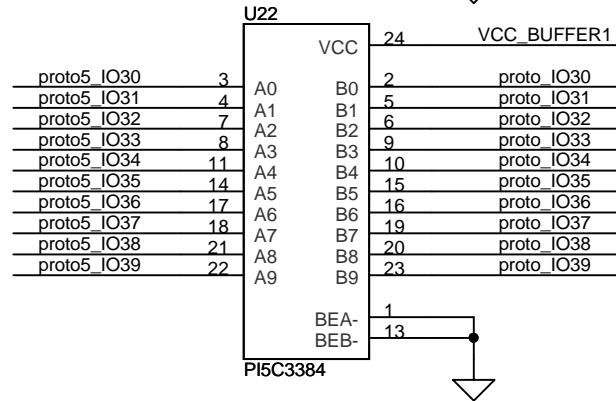
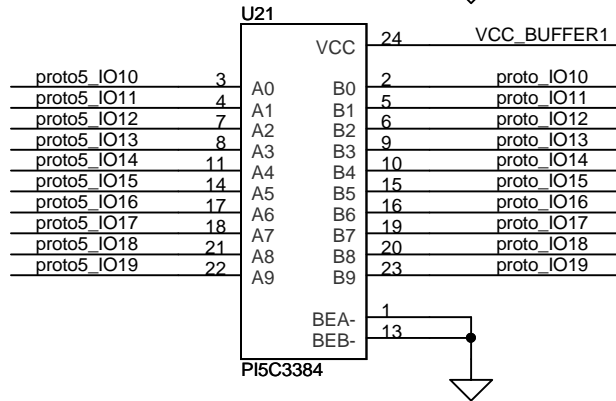
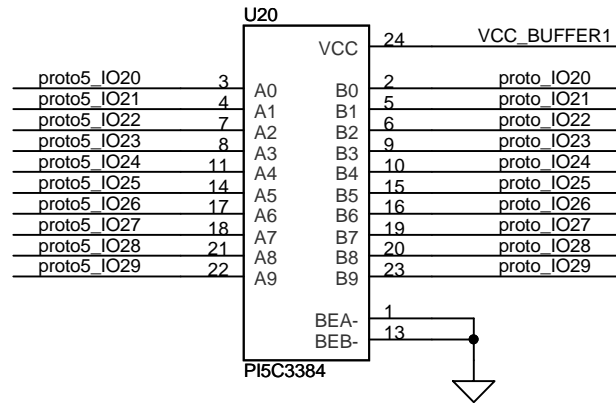
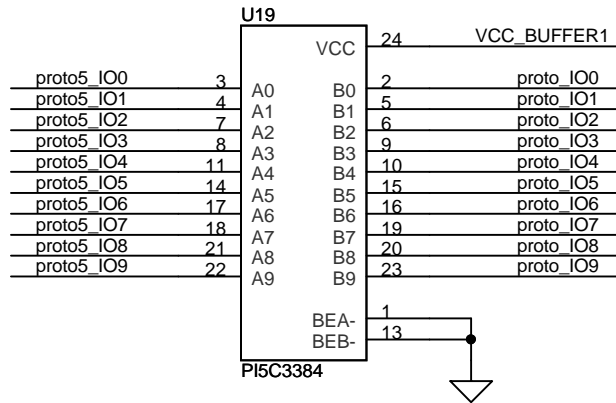
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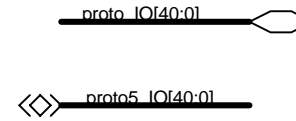
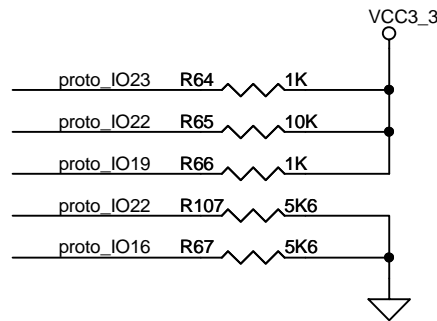
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NO CHANGE

Protol Buffers

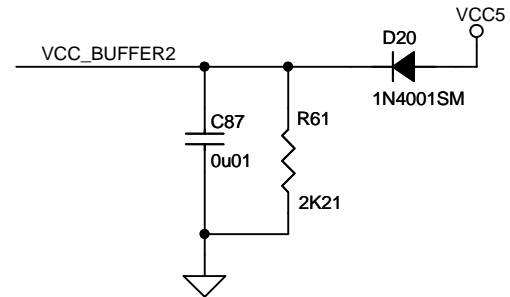
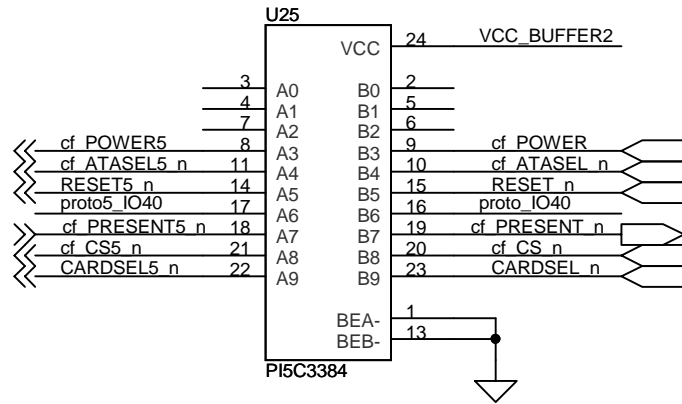


R65 and R107 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R65 should be a nostuff for production.



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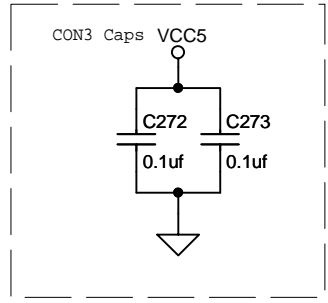
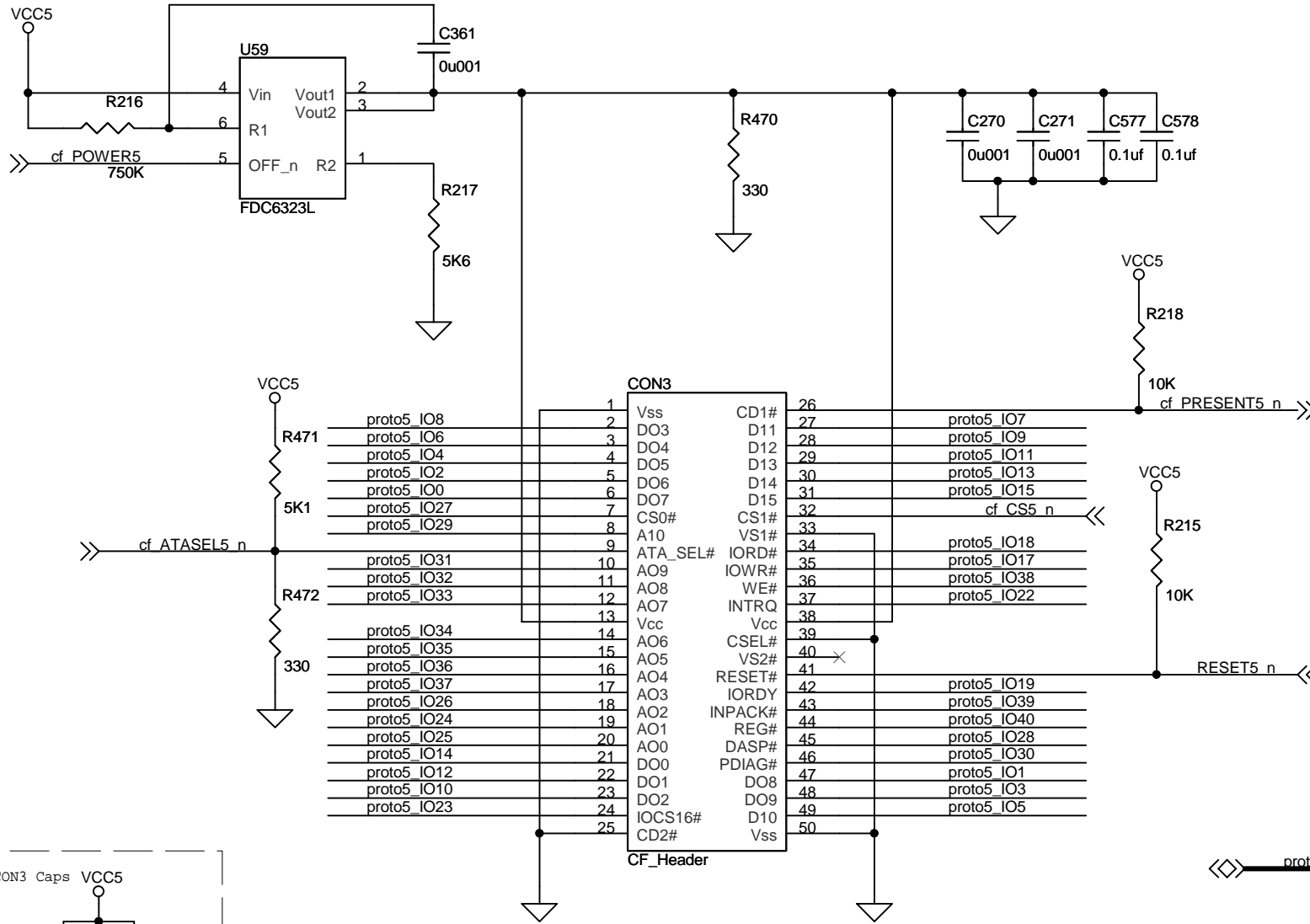
NO CHANGE



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NO CHANGE

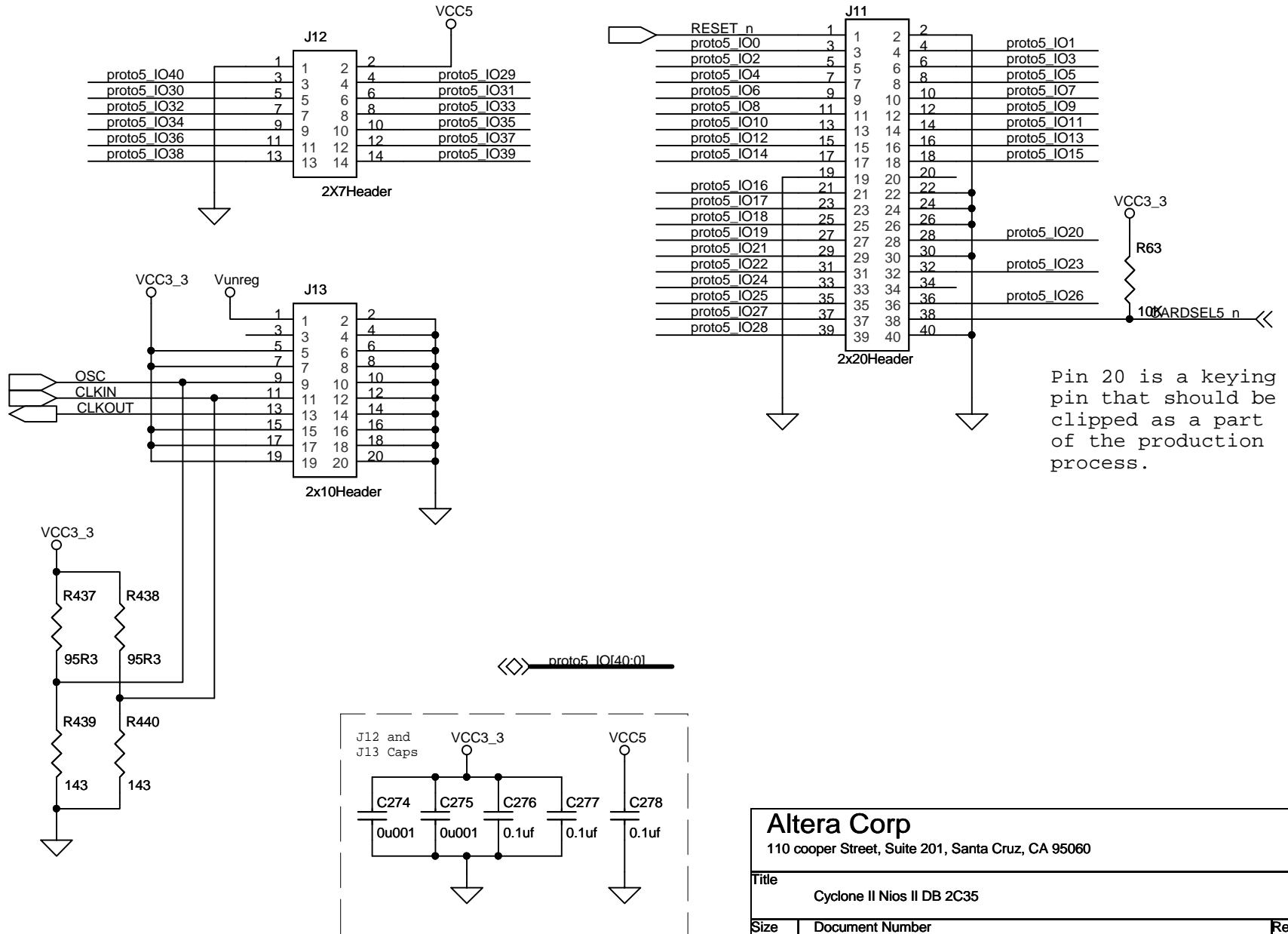
Compact Flash Socket



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NO CHANGE

Protocard 1

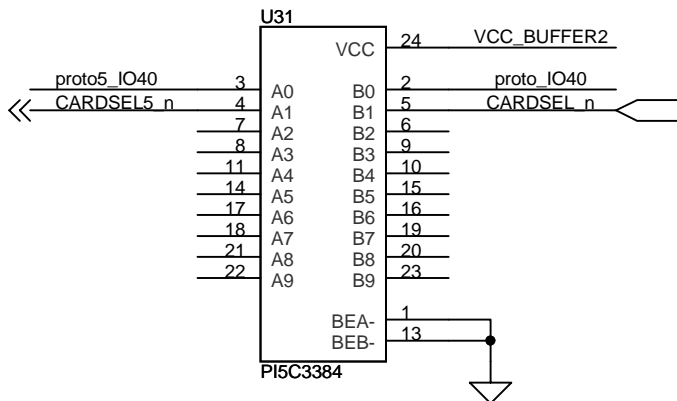
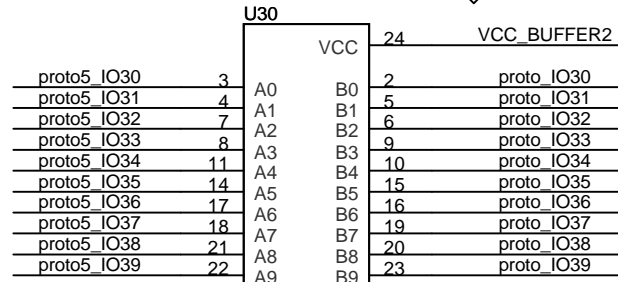
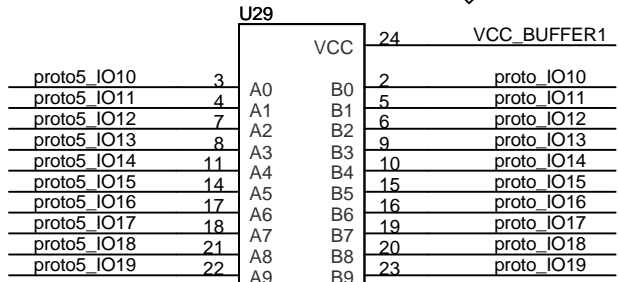
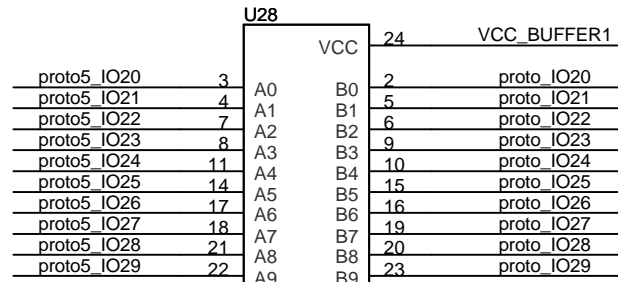
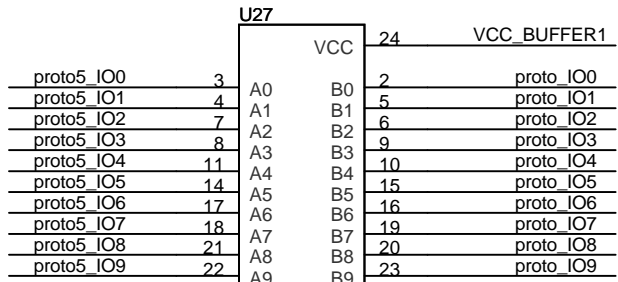


Pin 20 is a keying pin that should be clipped as a part of the production process.

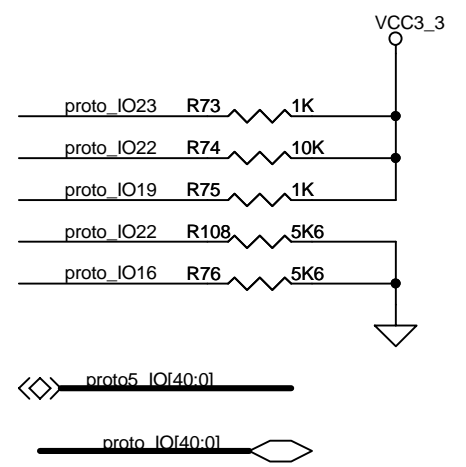
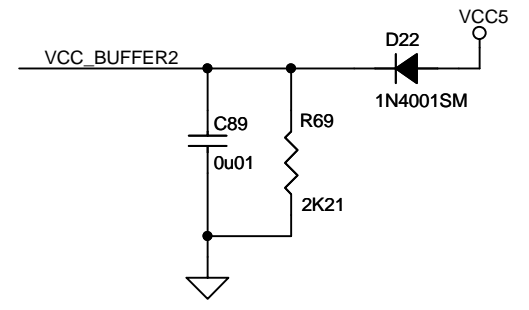
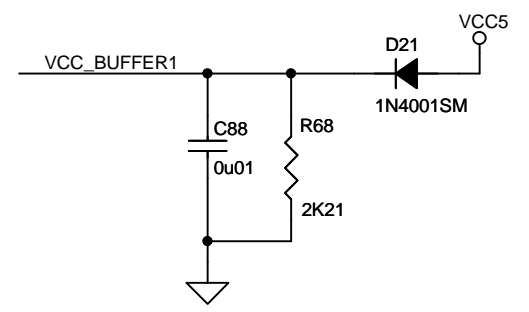
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NO CHANGE

Proto2 Buffers



R74 and R108 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R74 should be a nostuff for production.



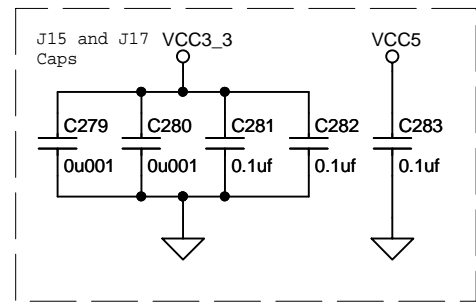
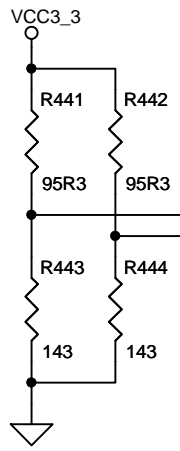
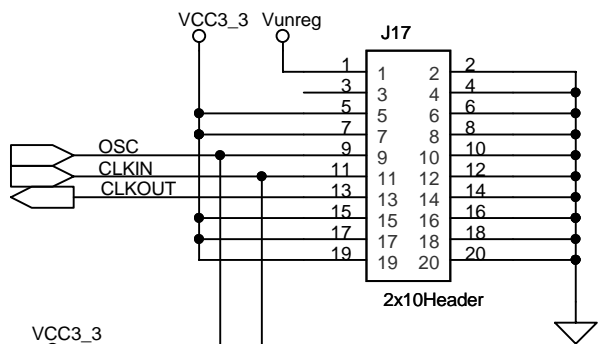
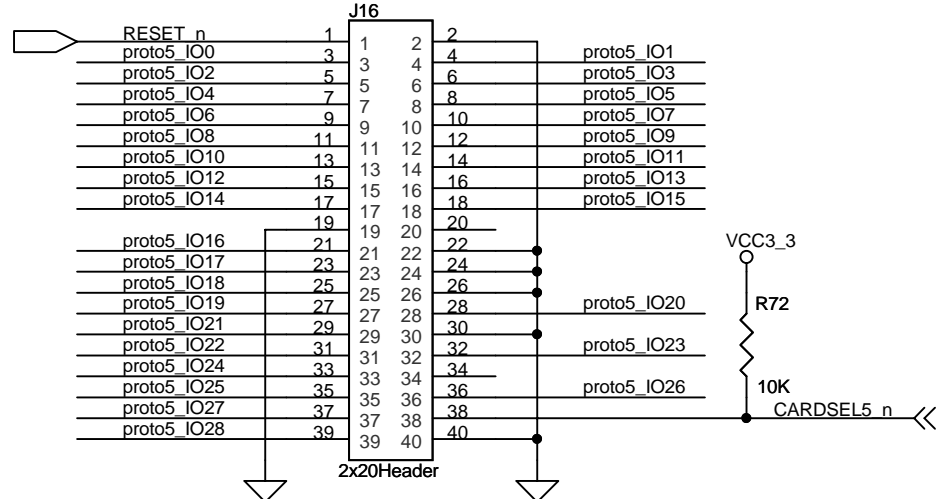
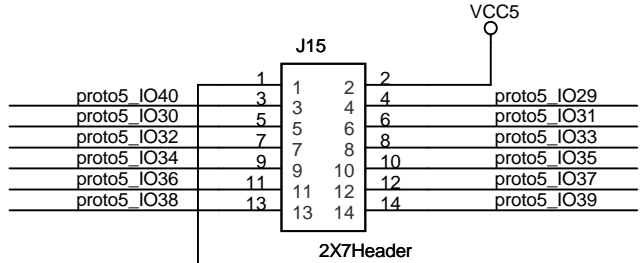
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NO CHANGE

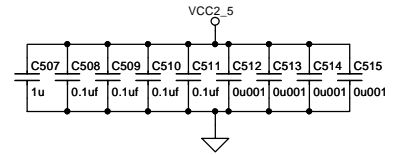
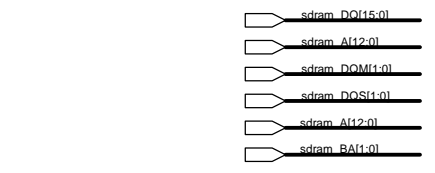
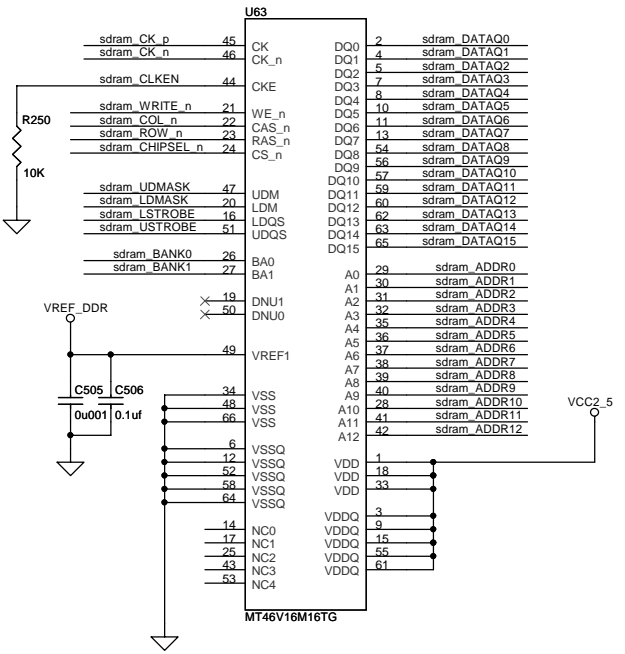
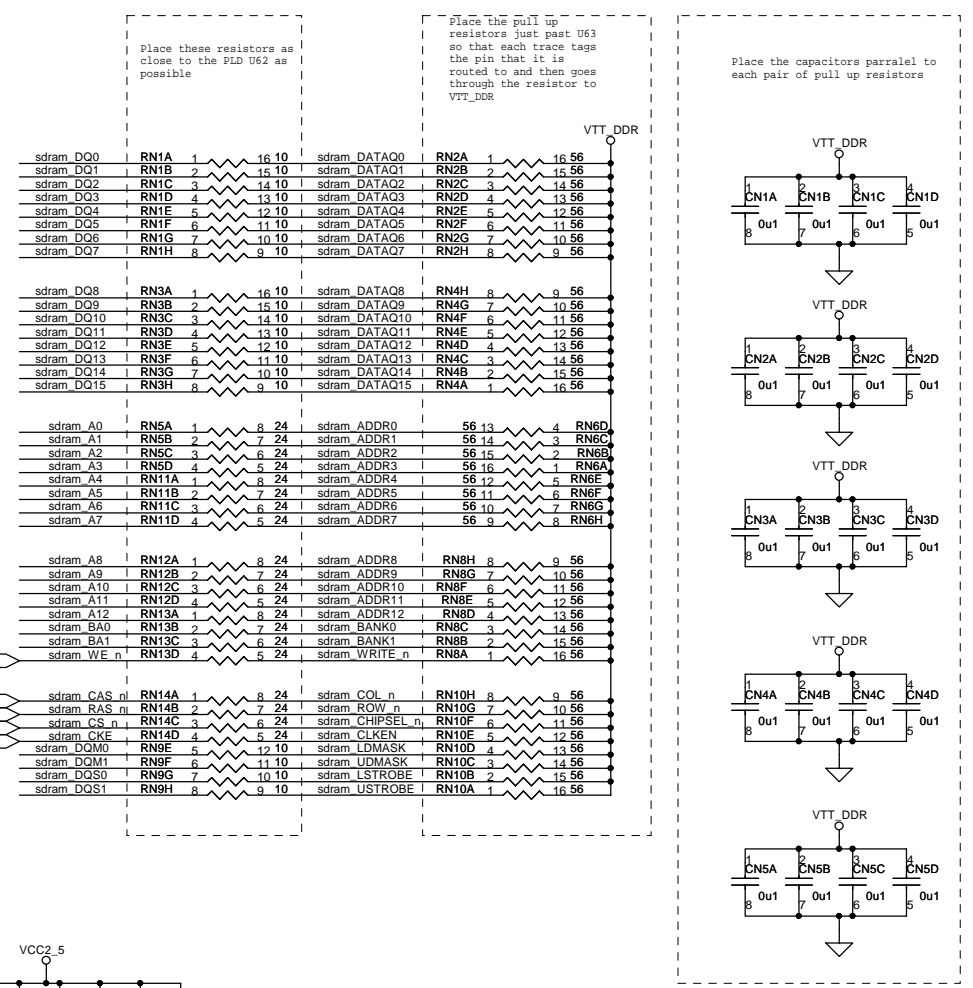
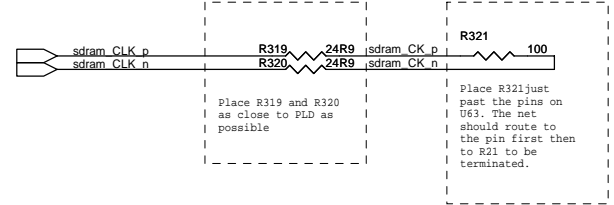
Proto2 Headers

◁ proto5 IO[40:0]

Pin 20 is a keying pin that should be clipped as a part of the production process.



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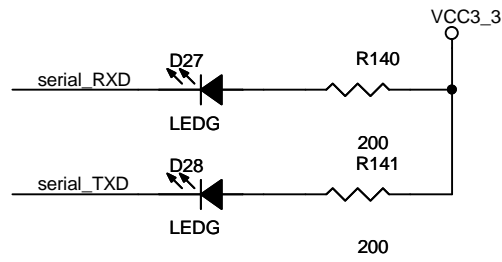
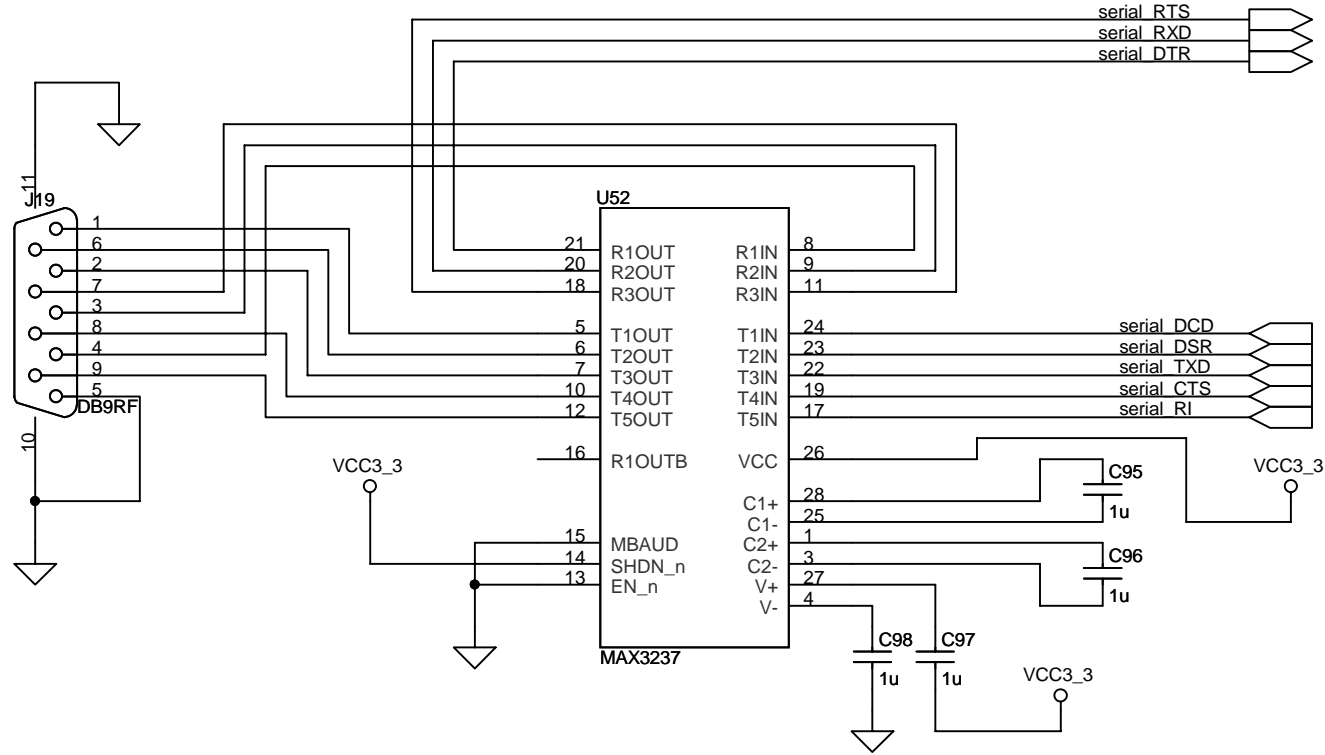
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Serial Ports



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5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

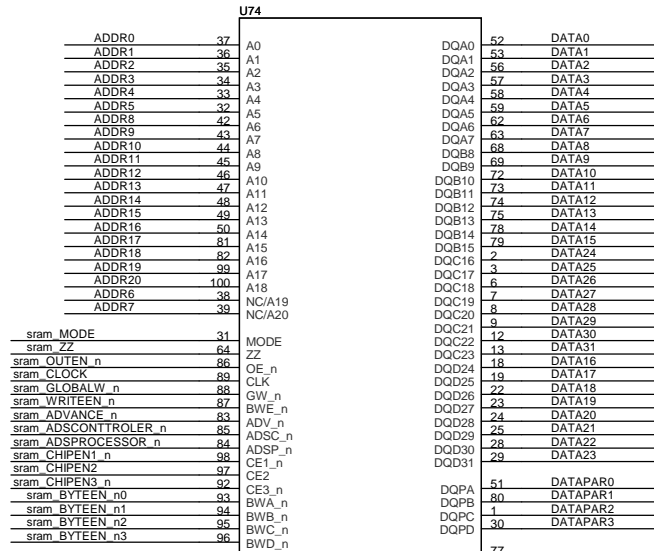
3

2

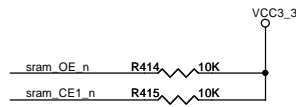
1

Note! ADDR6 and ADDR7 are only used when using the larger memory chips. They are connected to the FPGA in the event that someone may want to use a larger chip.

Note! The data bus was pinned out on the rev 01 board such that the C byte and D byte were swapped. This can be rectified by swapping the C and D byte in your quartus project.



One bank of 512K x 36 SRAM 2Mbyte of SRAM



DATA0	RN15A	1	8	24	D0
DATA1	RN15B	2	7	24	D1
DATA2	RN15C	3	6	24	D2
DATA3	RN15D	4	5	24	D3
DATA4	RN16A	1	7	24	D4
DATA5	RN16B	2	6	24	D5
DATA6	RN16C	3	5	24	D6
DATA7	RN16D	4	4	24	D7
DATA8	RN17A	1	8	24	D8
DATA9	RN17B	2	7	24	D9
DATA10	RN17C	3	6	24	D10
DATA11	RN17D	4	5	24	D11
DATA12	RN18A	1	8	24	D12
DATA13	RN18B	2	7	24	D13
DATA14	RN18C	3	6	24	D14
DATA15	RN18D	4	5	24	D15
DATA16	RN19A	1	8	24	D16
DATA17	RN19B	2	7	24	D17
DATA18	RN19C	3	6	24	D18
DATA19	RN19D	4	5	24	D19
DATA20	RN20A	1	8	24	D20
DATA21	RN20B	2	7	24	D21
DATA22	RN20C	3	6	24	D22
DATA23	RN20D	4	5	24	D23
DATA24	RN21A	1	8	24	D24
DATA25	RN21B	2	7	24	D25
DATA26	RN21C	3	6	24	D26
DATA27	RN21D	4	5	24	D27
DATA28	RN22A	1	8	24	D28
DATA29	RN22B	2	7	24	D29
DATA30	RN22C	3	6	24	D30
DATA31	RN22D	4	5	24	D31
DATAPAR0	RN23A	1	8	24	DP0
DATAPAR1	RN23B	2	7	24	DP1
DATAPAR2	RN23C	3	6	24	DP2
DATAPAR3	RN23D	4	5	24	DP3

Place these terminations in the middle of the line

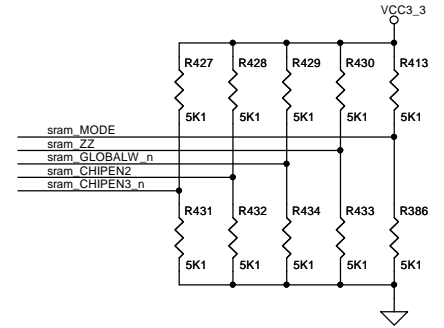
ADDR0	RN24A	1	8	24	A0
ADDR1	RN24B	2	7	24	A1
ADDR2	RN24C	3	6	24	A2
ADDR3	RN24D	4	5	24	A3
ADDR4	RN25A	1	8	24	A4
ADDR5	RN25B	2	7	24	A5
ADDR6	RN25C	3	6	24	A6
ADDR7	RN25D	4	5	24	A7
ADDR8	RN26A	1	8	24	A8
ADDR9	RN26B	2	7	24	A9
ADDR10	RN26C	3	6	24	A10
ADDR11	RN26D	4	5	24	A11
ADDR12	RN27A	1	8	24	A12
ADDR13	RN27B	2	7	24	A13
ADDR14	RN27C	3	6	24	A14
ADDR15	RN27D	4	5	24	A15
ADDR16	RN28A	1	8	24	A16
ADDR17	RN28B	2	7	24	A17
ADDR18	RN28C	3	6	24	A18
ADDR19	RN28D	4	5	24	A19
ADDR20	RN29A	1	8	24	A20

Place these terminations near U62

sram_BYTEEN_n0	RN29B	2	7	24	sram_BE_n0
sram_BYTEEN_n1	RN29C	3	6	24	sram_BE_n1
sram_BYTEEN_n2	RN29D	4	5	24	sram_BE_n2
sram_BYTEEN_n3	RN30A	1	8	24	sram_BE_n3

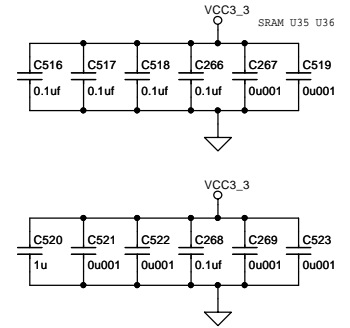
sram_OUTEN_n	RN30B	2	7	24	sram_OE_n
sram_CLOCK	RN30C	3	6	24	sram_CLK
sram_GLOBALW_n	RN30D	4	5	24	sram_GW_n
sram_WRITEEN_n	RN31A	1	8	24	sram_WF_n
sram_ADVANCE_n	RN31B	2	7	24	sram_ADV_n
sram_ADSCONTROLLER_n	RN31C	3	6	24	sram_ADSC_n
sram_ADSPROCESSOR_n	RN31D	4	5	24	sram_ADSP_n
sram_CHIPEN1_n	RN32A	1	8	24	sram_CE1_n
sram_CHIPEN2_n	RN32B	2	7	24	sram_CE2_n
sram_CHIPEN3_n	RN32C	3	6	24	sram_CE3_n

SRAM



Default SRAM Settings

sram_MODE = Linear Burst (GND NOSTUFF R413)
sram_ZZ = Always Enabled (GND NOSTUFF R430)
sram_GLOBALW_n = Global Write Disable (VCC NOSTUFF R434)
sram_CHIPEN2 = Always Enabled (VCC NOSTUFF R432)
sram_CHIPEN3_n = Always Enabled (GND NOSTUFF R427)



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